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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,583	12/21/2000	Daniel Leibholz	SMQ-023	3889

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,583	LEIBHOLZ ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 3/4/2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin U.S. Patent Number 6,631,452 (as applied in the previous Office Action).

5. Referring to claim 1, Lin has taught a microprocessor, comprising:

a) registers for holding values, wherein said registers are logically partitioned into register windows (Lin figure 2, figure 4, column 4 lines 1-29; the frames are the register windows);

b) a storage for storing values held in the registers of the register windows (Lin figure 2, figure 4, column 4 lines 1-29; the backing store);

c) a detector for detecting that one of a register window overflow condition and a register window underflow condition is imminent (Lin column 8 line 49-column 9 line 5, figure 6; the mandatory fill and spill operations come from underflow and overflow conditions); and

d) an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap performing at least one of a register window spill operation or a register window fill operation responsive to the condition that is detected as imminent (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract). It should be noted that the purpose of successfully performing speculative spills/fills is to eliminate the need for performing mandatory spills/fills. See column 5, line 42, to column 6, line 2. In the case when a speculative spill/fill is successful, the mandatory spill/fill would be unnecessary as the speculative spill/fill has already completed the task to be performed by the mandatory spill/fill. This prevents the stall associated with the mandatory spill/fill from being incurred. When a speculative spill/fill is successful, then the associated mandatory spill/fill is avoided. This is clearly Lin's intention as the purpose of Lin's system is to reduce stalls associated with mandatory spills/fills.

6. Referring to claim 2, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the detector and the instruction generator are implemented in hardware (Lin column 11 lines 1-15).

7. Referring to claim 3, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the microprocessor further comprises a cache for caching instructions (Fig.1, component 130) for introduction into an execution stage and wherein the detector examines the instructions in the cache to determine if a register window overflow condition is imminent by

determining if execution of any of the fetched instructions will result in a register window overflow condition. See Fig.6 and column 8, line 58, to column 9, line 63. The instructions in the cache are the same instructions that are to be executed. No matter what point the instructions are monitored, they are "the instructions in the cache". That is, applicant is not claiming that the instructions are monitored while in the cache and before being fetched from the cache for decoding, execution, etc. Applicant merely claims monitoring instructions in the cache and an instruction that is being executed is also an instruction in the cache as that is where it was fetched from.

8. Referring to claim 4, Lin has taught a microprocessor as described in claim 3. Lin has further taught that the detector looks for an instruction in the cache that stores contents of a register window in the registers when the registers have no available space for storing the contents (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 6, column 8 line 49-column 9 line 5).

9. Referring to claim 5, Lin has taught a microprocessor as described in claim 3. Lin has further taught that the detector examines how much storage space is available in the registers (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 6, column 8 line 49-column 9 line 5).

10. Referring to claim 6, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the microprocessor further comprises a cache for caching instructions for introduction into an execution stage and wherein the detector examines the instructions in the cache to determine if a register window underflow condition is imminent by determining if execution of the instructions will result in a register window underflow condition. See Fig.6 and

column 8, line 58, to column 9, line 63. The instructions in the cache are the same instructions that are to be executed. No matter what point the instructions are monitored, they are "the instructions in the cache". That is, applicant is not claiming that the instructions are monitored while in the cache and before being fetched from the cache for decoding, execution, etc. Applicant merely claims monitoring instructions in the cache and an instruction that is being executed is also an instruction in the cache as that is where it was fetched from.

11. Referring to claim 7, Lin has taught a microprocessor as described in claim 6. Lin has further taught that the detector looks for an instruction in the cache that restores a register window when contents of the register window are stored on the stack rather than in the registers (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 6, column 8 line 49-column 9 line 5).

12. Referring to claim 8, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the detector detects solely whether a register window underflow condition is imminent (Lin column 11 lines 40-43).

13. Referring to claim 9, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the detector detects solely whether a register window overflow condition is imminent (Lin column 11 lines 35-39).

14. Referring to claim 10, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the detector detects both whether a register window overflow condition is imminent and whether a register window underflow condition is imminent (Lin column 8 line 49-column 9 line 5, figure 6; the mandatory fill and spill operations come from underflow and overflow conditions).

15. Referring to claim 11, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the microprocessor further comprises an execution unit for executing the instruction generated by the instruction generator (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 4).

16. Referring to claim 12, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the microprocessor performs out of order execution of instructions (Lin column 3 lines 32-45; speculative processing by definition is not a certain operation, but is a prediction based on some information, and because of a misprediction, the wrong order of operations will occur).

17. Referring to claim 13, Lin has taught a microprocessor as described in claim 1. Lin has further taught that the instruction generator includes a second storage for holding the at least one instruction that is generated by the instruction generator (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract; it is inherent that some ROM or other memory would be available to hold the speculative operations, that the RSE chooses to executes).

18. Referring to claim 14, Lin has taught in a microprocessor having a storage and registers, an engine, comprising:

a) a detector for detecting that a trap requiring an access to the storage to manage register window information is imminent (Lin column 8 line 49-column 9 line 5, figure 6; the mandatory fill and spill operations come from underflow and overflow conditions).

b) an instruction generator responsive to the detector for generating at least one instruction to avoid the trap performing at least one of a register window spill operation or a register window fill operation (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2,

abstract). It should be noted that the purpose of successfully performing speculative spills/fills is to eliminate the need for performing mandatory spills/fills. See column 5, line 42, to column 6, line 2. In the case when a speculative spill/fill is successful, the mandatory spill/fill would be unnecessary as the speculative spill/fill has already completed the task to be performed by the mandatory spill/fill. This prevents the stall associated with the mandatory spill/fill from being incurred. When a speculative spill/fill is successful, then the associated mandatory spill/fill is avoided. This is clearly Lin's intention as the purpose of Lin's system is to reduce stalls associated with mandatory spills/fills.

19. Referring to claim 15, Lin has taught a microprocessor as described in claim 14. Lin has further taught that the engine is implemented in hardware. See column 11, lines 1-15.

20. Referring to claim 16 Lin has taught a microprocessor having a plurality of registers logically partitioned into register windows and a storage for storing contents of register windows, a method, comprising the steps of:

a) determining that one of a register window overflow condition and a register window underflow condition is imminent (Lin column 8 line 49-column 9 line 5, figure 6, column 5 line 46-column 6 line 2, abstract; the mandatory fill and spill operations come from underflow and overflow conditions); and

b) in response to determining that the one of the register overflow condition and register window underflow condition is imminent, manipulating the storage to avoid a trap performing at least one of a register window spill operation or a register window fill operation responsive to the condition determined as imminent (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract). It should be noted that the purpose of successfully performing

speculative spills/fills is to eliminate the need for performing mandatory spills/fills. See column 5, line 42, to column 6, line 2. In the case when a speculative spill/fill is successful, the mandatory spill/fill would be unnecessary as the speculative spill/fill has already completed the task to be performed by the mandatory spill/fill. This prevents the stall associated with the mandatory spill/fill from being incurred. When a speculative spill/fill is successful, then the associated mandatory spill/fill is avoided. This is clearly Lin's intention as the purpose of Lin's system is to reduce stalls associated with mandatory spills/fills.

21. Referring to claim 17, Lin has taught a method as described in claim 16. Lin has further taught that when it determined that a register window overflow condition is imminent, the step of manipulating the storage comprises providing at least one instruction for execution by the microprocessor that causes the contents in at least the selected register window to be stored in the storage (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract).

22. Referring to claim 18, Lin has taught a method as described in claim 16. Lin has further taught that when it is determined that a register window underflow condition is imminent, the step of manipulating the storage comprises providing at least one instruction for execution by the microprocessor that causes data in the storage to be stored in the registers (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract).

23. Referring to claim 19, Lin has taught a method as described in claim 16. Lin has further taught that the microprocessor has an instruction stream slated for execution and wherein the instruction that causes the contents in at least the selected register window to be stored in the storage is inserted into the instruction stream (Lin column 7 line 45-column 8 line 15, column 5

line 46-column 6 line 2, abstract, figure 4; the instruction stream is the operations in figure 4 that spill and fill the registers from memory).

Response to Arguments

24. Applicant's arguments filed on March 4, 2005, have been fully considered but they are not persuasive.

25. Applicant argues the novelty/rejection of claims 1, 14, and 16 on page 6 of the remarks, in substance that:

> "Lin discloses that the speculative spill/fill operations reduce the need for the mandatory spill/fill operations. Lin, however, does not disclose that the processor avoids a trap performing one of a register window spill operation or a register window fill operation...Although the need for the mandatory spill/fill operation is reduced in Lin, the mandatory spill/fill operation is still required if RSE-related instructions (RI) are monitored and registers are not available in the register stack."

26. These arguments are not found persuasive for the following reasons:

a) The examiner admits that mandatory spill/fill operations are not completely avoided. In fact, the use of mandatory spill/fill operations is clearly shown in Fig.6 and in Table 2 shown in column 8. However, this does not mean that mandatory operations aren't avoided sometimes. It should be noted that the purpose of successfully performing speculative spills/fills is to eliminate the need for performing mandatory spills/fills. See column 5, line 42, to column 6, line 2. In the case when a speculative spill/fill is successful, the mandatory spill/fill would be unnecessary as the speculative spill/fill has already completed the task to be performed by the mandatory spill/fill. This prevents the stall associated with the mandatory spill/fill from being incurred. When a speculative spill/fill is successful, then the associated mandatory spill/fill is avoided. This is clearly Lin's intention as the purpose of Lin's system is to reduce stalls associated with mandatory spills/fills. Even if applicant is correct in saying that mandatory operations are not

avoided in a certain situation, the examiner is also correct in saying that mandatory operations are avoided in a certain situation. Consequently, this limitation is still taught. For instance, if applicant claims performing an operation "A" and the prior art discloses performing operations "A" and "B", then performing operation "A" is still taught regardless of the existence of performing operation "B".

27. Applicant argues the novelty/rejection of claims 3 and 6 on page 7 of the remarks, in substance that:

> "Applicants submit that Lin fails to teach or suggest that the detector examines the instructions in the cache, as recited in claims 3 and 6. In the Office action, the Examiner notes that the instruction in the cache can be examined when they make their way into the pipeline and the execution unit, which is taught in Lin. As the Examiner notes in the Office Action, Lin teaches monitoring instructions, such as RI, in the pipeline and the execution unit. Lin does not teach that the detector examines the instructions in the cache."

28. These arguments are not found persuasive for the following reasons:

a) Instructions are stored in instruction cache 130 of Fig.1. They are then fetched from the instruction cache to be decoded and eventually executed. Therefore, all instructions, at any point during the execution process, are instructions in the cache, as that is where they originated, and still exist. That is, regardless of when they are monitored, which is not explicitly disclosed by Lin, the instructions are instructions in the cache. Applicant is not claiming when the instructions are monitored (while instructions are in the cache and before they're fetched, for instance, if that is what applicant is in fact doing (and has support in the specification for)). Instead, applicant is merely claiming monitoring instructions in the cache which is done by Lin at some point in time.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
May 10, 2005

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